ISSN 2348 – 9928
IJAICT Volume 4, Issue 1, January 2017 Doi:01.0401/ijaict.2014.07.18 Published on 05 (1) 2017

DESIGN AND SIMULATION OF 64 BIT DIVIDER USING VEDIC MATHEMATICS

Miss. Aditi S.Tadas
PG Scholar – VLSI,
G.H,Raisoni Institute of Engineering and Technology for Womens,
Nagpur, India

Prof. Dinesh Rotake
Department of Electronics & Telecommunication,
G.H,Raisoni Institute of Engineering and Technology for Womens,
Nagpur, India

Abstract— The idea for designing the Divider unit is adopted from ancient Indian mathematics "Vedas" .Vedic Mathematics is the old method of computing. With the advent of new technology in the fields of VLSI and communication, there is also an always increasing demand for high speed processing and low area design. Divider is an important fundamental function in arithmetic operations. It is also known fact that the Divider unit forms an integral part of processor design. Due to this regard, high speed Divider architectures become the need of the day. In this, we introduce a performance of the device with various methods of Vedic Mathematics .The methods used in this are faster than the Normal methods of Division. The functionality of these circuits was checked and performance parameters were calculated. The design and experiments were carried out on a Xilinx and implementation of FPGA and the timing and area of the design, on the same parameters have been calculated.

Keywords— Nikhilam Navatascaramam Dasatah (NND), Paravartya Yojayet, Flagpole (Dhvajanka), Vedic Mathematics.

I. INTRODUCTION

Binary Division as the name has its unique importance in the field of hardware implementation of signal processing where high qualities of Graphics are processed, DSP applications. As we know division operation is not combinational operation but it's a sequential kind of operation and hence it is costly then other type of Arithmetic Operation that is Multiplication and Addition [1].

In Algorithmic and Structural Levels, a lot of Division techniques have been developed to reduce various important factors including the factors like Latency, Propagation delay, computational Time Division is one of the important arithmetic operations in such applications and development of fast division circuit has [4][5] been a subject of interest over decades. Among the remaining methods, Vedic Mathematics is the ancient system of Indian mathematics which is based on Vedas which means 'Store House of Knowledge' which has a unique technique of calculations based on 16 Sutras (Formulae) and 13 corollaries. Vedic Mathematics offers a new and completely dissimilar approach to the Study of Mathematics based on pattern recognition. Vedic Mathematics is Monumental Work done by (Bharti Krishna Tirtha) Shankaracharya. He was Master in numerals.

In this paper division is based on such ancient Methods of calculation. "Nikhilam Navatascaramam Dasatah" (NND) is a Sanskrit term indicating "all from 9 and last from 10", Paravartya Yojayet"Transpose and Apply" , Flagpole are adopted from Vedas; formulae are encountered to implement the division circuitry. By employing the Vedic methodology, division has been implemented by multiplication addition and subtraction, therefore reduces the iteration, owing to the substantial reduction in propagation delay.

II. LITERATURE SURVEY

To know the state-of-art in technology, a literature survey is carried out related to Division carried out with the help of Vedic Mathematics. Divider can be designed as per the need. Prabir Saha, Arindam Banerjee, Partha Bhattacharyya and Anup Dandapat[1] have performed division Using Nikhilam Navatascaramam Dasatah (NND*)* sutra in the paper "Vedic Divider: Novel Architecture (ASIC) for High Speed VLS Applications", 2011 International Symposium on Electronic System Design. In this paper, 16 bit dividend by 8 bit divisor architecture based on one of the sutra of ancient Vedic Mathematics

Again by using another sutra Division is performed by Soma BhanuTej [2]. "Vedic Divider - A High Performance Computing algorithm for VLSI Applications", in this paper the Vedic divider implemented using Paravartya-yojayet (PYY) sutra of different configuration is compared with conventional Division implemented divider. In this paper Division is performed which is having the Dividend of 32 bit and divisor is of 16 bit.

ISSN 2348 – 9928
Doi:01.0401/ijaict.2014.07.18 Published on 05 (1) 2017

Another Division is again performed using the another Vedic Mathematics method that is Dhavjanka sutra by R.Thamil Chelvani, S.Roobini Priya[3] " Implementation of Fixed and floating point Division using Dhavajanka sutra" Vol 04, Issue 02; March - April 2013 International Journal of VLSI and Embedded Systems-IJVES.This paper proposes the implementation of RSA encryption/ decryption algorithm using the algorithms of Ancient Indian Vedic mathematics that has been modified to improve the performance.

According to Literature Survey, it is Observed that fewer work is done in the area of Vedic Mathematics. The Existing Methods are combined and this method is proposed Which will be definitely the great work for the division.

III. PROPOSED WORK

In this paper division algorithm and its architecture based on such ancient Indian arithmetic. "Nikhilam Navatascaramam Dasatah" (NND) is a Sanskrit term representing "all from 9 and last from 10", Paravartya Yojayet which means "Transpose and Apply", Flagpole are adopted from Vedas; formulae are encountered to implement the division circuitry. By employing the Vedic methodology, division has been implemented by multiplication addition and subtraction, therefore reduces the iteration, owing to the substantial reduction in propagation delay.The Flow Chart for the Proposed Design is Shown Below.

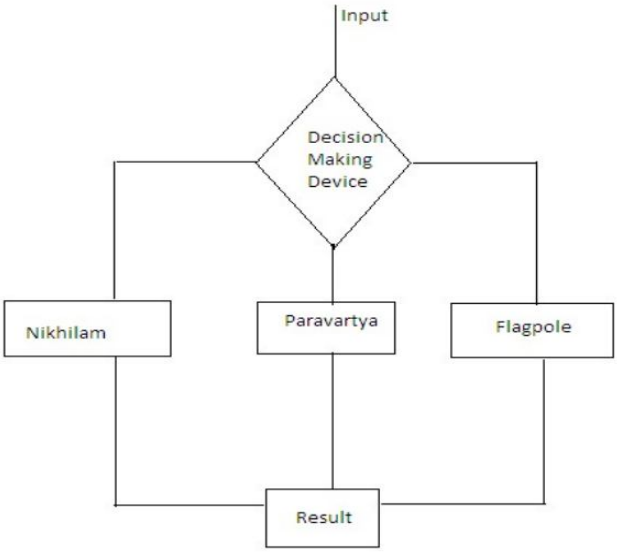

Fig : 1 Flow chart of Proposed Plan

IV. CONCLUSION

This Methods (sutras/Formulae) that are used in Dividing are more simple and faster, this is so because the Vedic formulae are based on the natural principles on which the human mind works, which increases the process speed, Helps in Fast Calculation and reduces power Issues. Vedic Divider will be implemented Using the three sutras namely NikhilamNavatascaramam Dasatah (NND), Paravartya Yojayet, Flagpole which is better than the normal Arithmetic Operation. This Methods(sutras/Formulaes) that are used in Dividing are more simple and faster, this is so because the Vedic formulae are based on the natural principles on which the individual mind works, which increases the process speed, helps in Fast Calculation and reduces power Issues.

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